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10/678,937	10/03/2003	James R. Spehar	US02 0121A	1189

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,937	SPEHAR, JAMES R.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the Applicant's preliminary amendment submitted on 10/03/2003. By virtue of this preliminary amendment, claims 1-20 are cancelled, claims 21-40 are newly added; thus claims 21-40 are pending in the instant application.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 21-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 5-6 and 8 of U.S. Patent No. 6,700,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skills in the art would recognize that the phrase *"a sync circuit, operably coupled between the first and the second paths, which is configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by dynamically synchronizing the two paths through the sync circuit"* (at the end of claim 21 of the instant application) is synonymous to the phrase *"a sync circuit, operably coupled between the first and the second*

paths, which is configured to synchronize the speed of signals traveling on the two paths" (toward the end of claim 1 of U.S. Patent No. 6,700,420).

3. Claims 21 and 29 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1of U.S. Patent No. 6,700,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skills in the art would recognize that the phrase *"the sync circuit dynamically synchronizes the two paths by slowing down a faster of the two paths arrive at the output driver at substantially a same time"* (claim 29 of the instant application) is synonymous to the phrase *"a sync circuit, operably coupled between the first and second paths, that is configured to synchronize the speed of signals traveling on the two paths"* (toward the end of claim 1 of U.S. Patent No. 6,700,420).

4. Claims 30-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 5-6 and 8 of U.S. Patent No. 6,700,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skills in the art would recognize that the phrase *"a sync circuit, operably coupled between the first and the second paths, which is configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bidirectionally synchronizing the two paths through the sync circuit"* (at the end of claim 30 of the instant application) is synonymous to the phrase *"a sync circuit, operably coupled between the first and the second paths, which is configured to synchronize the speed of signals traveling on the two paths"* (toward the end of claim 1 of U.S. Patent No. 6,700,420).

5. Claims 30 and 38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1of U.S. Patent No. 6,700,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skills in the art would recognize that the phrase *"the sync circuit dynamically synchronizes the two paths by slowing down a faster of the two paths arrive at the output driver at substantially a same time"* (claim 30 of the instant application) is synonymous to the phrase *"a sync circuit, operably coupled between the first and second paths, that is configured to synchronize the speed of signals traveling on the two paths"* (toward the end of claim 1 of U.S. Patent No. 6,700,420).

6. Claim 39 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,700,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because one of ordinary skills in the art would recognize that the phrase *"a sync circuit, operably coupled between the first and the second paths, which is configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bidirectionally synchronizing the two paths through the sync circuit to slow a faster of the two paths"* (claim 39 of the instant application) is synonymous to the phrase *"a sync circuit, operably coupled between the first and second paths, that is configured to synchronize the speed of signals traveling on the two paths"* (toward the end of claim 1 of U.S. Patent No. 6,700,420).

7. Claims 39 and 40 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,700,420. Although the conflicting claims are not identical, they are not patentably distinct from each other because one

of ordinary skills in the art would recognize that the phrase *"the faster of the two paths is slowed such that the signals of the two paths arrive at the output driver at substantially at a same time"* (claim 40 of the instant application) is synonymous to the phrase *"a sync circuit, operably coupled between the first and second paths, that is configured to synchronize the speed of signals traveling on the two paths"* (toward the end of claim 1 of U.S. Patent No. 6,700,420).

Claim Objections

8. Claims 24, 26 and 30 are objected to because of the following informalities:

Claim 24, line 4, delete extra space after "and".

Claim 26, line 2, insert -- . -- at end of line.

Claim 30, line 11, change "synch" to --sync-- is suggested to be consistent with "sync" in line 9.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 21-24 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1) in view of Huber et al. (U.S. Patent No. 6,420,920).

With respect to claims 21 and 29, the Applicant's Admitted Prior Art (Fig. 1) discloses a differential output structure comprising (1) an input line including (i) a first path [Path 1] having an input end *(common node besides A)* for receiving an input signal *(coming from A)*, an output

end [D], and including driving elements [12, 16, 18], and (ii) a second path [Path 2] having an input end *(common node besides A)* operably coupled to the input end of the first path for receiving the input signal *(coming from A)*, and an output end; and (2) an output driver [32], which is (i) operably coupled to the output ends of the first and second paths, and (ii) configured to provide differential outputs [M, N].

The Applicant's Admitted Prior Art (Fig. 1) lacks a sync circuit, which is (i) operably coupled between the first and second paths, and (ii) configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by dynamically synchronizing the two paths through the sync circuit and by slowing down a faster of the two paths such that the signals of the two paths arrive at the output driver at substantially a same time.

Huber et al. discloses, in Fig. 3, a sync circuit [60], which is (i) operably coupled between first and second paths [42, 44], and (ii) configured to synchronize the speed of signals traveling on the two paths [42, 44] *(by regulating slew rates of the signals; see col. 4, lines 63-67; col. 5, lines 1-12)*.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the differential output structure of the Applicant's Admitted Prior Art (Fig. 1) by additionally configuring a sync circuit between the first and second paths of the differential output structure of the Applicant's Admitted Prior Art (Fig. 1) to provide an increase in the slew rate and thus to synchronize the speed of signals traveling on the two paths, since such an arrangement of the sync circuit for the stated purpose has been a well known practice in the art as evidenced by the teachings of Huber et al. *(see Huber et al.; col. 4, lines 63-67; col. 5, lines 1-12)*.

With respect to claim 22, Fig. 1 of the Applicant's Admitted Prior Art discloses that (1) the first path further includes a plurality of driving elements [12, 16, 18] connected in series to one another, and provides an inverted *(inverted/non-inverted is counted through inverters 12, 16, 18)* output [D] of the input signal, and (2) the second path includes a plurality of driving elements [26, 28] being connected in series to one another, and provides a non-inverted *(inverted/non-inverted is counted through inverters 12, 16, 18)* output [F] of the input signal.

With respect to claim 23, the Applicant Admitted Prior Art (Fig. 1) discloses that the driving elements of the first (12, 16, 18) and second (26, 28) paths have a predetermined constant taper ratio *(indicated in the driving elements).*

With respect to claim 24, the Applicant Admitted Prior Art (Fig. 1) discloses that each sync circuit is coupled between an output of a driving element on the first path having a first current driving capability and an output of a driving element on the second path having a second current driving capability, and wherein the first current driving capability is greater than the second current driving capability.

With respect to claim 27, the combination of Applicant Admitted Prior Art (Fig. 1) and Hubert et al. discloses that each of the sync circuits includes a capacitance. *As indicated in rejection for claim 21, Hubert et al. discloses the sync circuit as an inverter and it is well known in the art that inverters do have capacitance (see U.S. 6,107,847, col.7, lines 31-32).*

With respect to claim 28, Huber et al. discloses, in Fig. 3, a sync circuit [60], which is (i) operably coupled between first and second paths [42, 44], and (ii) configured to synchronize the speed of signals traveling on the two paths [42, 44] *(by regulating slew rates of the signals; see col. 4, lines 63-67; col. 5, lines 1-12).* Fig. 3 of Huber et al. does not show that the sync circuit

[60] is coupled between the output ends of the first and second paths. However, as shown in Fig. 3 of Huber et al., the sync circuit [60] affects the slew rate or speed of the signals on the two paths before the inputs of the inverters [48] and [54]. In other words, it would slow down the speed of the signal through the inverters [46, 64] so as to synchronize with the other signal that goes through the inverters [50, 66, 52] *(since the speed of the signal going through these inverters is slower than that in the other path as having more inverters or delay elements)* at the outputs. The inverters [48] and [54] are configured to receive the signals with equal speed after being regulated by the sync circuit [60]; and thus, they are not necessary in playing role in synchronizing the speed of the signals at the outputs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the differential output structure of the Applicant's Admitted Prior Art (Fig. 1) by additionally configuring a sync circuit between the output ends of the first and second paths of the differential output structure of the Applicant's Admitted prior Art (Fig. 1) to provide an increase in the slew rate and thus to synchronize the speed of signals traveling on the two paths, since such an arrangement of the sync circuit for the stated purpose has been a well known practice in the art as evidenced by the teachings of Huber et al. *(see Huber et al.; col. 4, lines 63-67; col. 5, lines 1-12).*

11. Claims 21, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1) in view of Parker et al. (U.S. Patent No. 5,375,148).

With respect to claims 21, 25 and 26, the Applicant's Admitted Prior Art (Fig. 1) discloses a differential output structure comprising (1) an input line including (i) a first path [Path 1] having an input end *(common node besides A)* for receiving an input signal *(coming*

from A), an output end [D], and including driving elements [12, 16, 18], and (ii) a second path [Path 2] having an input end *(common node besides A)* operably coupled to the input end of the first path for receiving the input signal *(coming from A)*, and an output end; and (2) an output driver [32], which is (i) operably coupled to the output ends of the first and second paths, and (ii) configured to provide differential outputs [M, N].

The Applicant's Admitted Prior Art (Fig. 1) lacks a) a sync circuit, which is (i) operably coupled between the output ends of the first and second paths, and (ii) configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by dynamically synchronizing the two paths through the sync circuit, and b) including another sync circuit and each sync circuit includes a capacitance.

Parker et al. discloses, in Fig. 2, a) a sync circuit [50], which is (i) operably coupled between first and second paths [(30,32,34, 36);(38,40, 42)], and (ii) configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bi-directionally synchronizing the two paths through the sync circuit *(by regulating the delay difference imposed by an unequal number of inverters; see col. 3, lines 22-52)*, and b) another sync circuit [54] and each sync circuit includes a capacitance that is included in the inverter.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the differential output structure of the Applicant's Admitted Prior Art (Fig. 1) by additionally configuring a sync circuit and an additional sync circuit between the first and second paths of the differential output structure of the Applicant's Admitted prior Art (Fig. 1) as taught by Parker et al. to overcome the delay difference imposed by an unequal number of inverters between the two paths since such an arrangement of the sync circuit for the

stated purpose has been a well known practice in the art as evidenced by the teachings of Parker et al. *(see Parker et al.; col. 3, lines 22-52).*

12. Claims 30-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art (Fig. 1) in view of Parker et al. (U.S. Patent No. 5,375,148).

With respect to claims 30, 34-36 and 38-40, the Applicant's Admitted Prior Art (Fig. 1) discloses a differential output structure comprising (1) an input line including (i) a first path [Path 1] having an input end *(common node besides A)* for receiving an input signal *(coming from A)*, an output end [D], and including driving elements [12, 16, 18], and (ii) a second path [Path 2] having an input end *(common node besides A)* operably coupled to the input end of the first path for receiving the input signal *(coming from A)*, and an output end; and (2) an output driver [32], which is (i) operably coupled to the output ends of the first and second paths, and (ii) configured to provide differential outputs [M, N].

The Applicant's Admitted Prior Art (Fig. 1) lacks a) a sync circuit, which is (i) operably coupled between the output ends of the first and second paths, and (ii) configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bi-directionally synchronizing the two paths and by slowing down a faster of the two paths such that the signals of the two paths arrive at the output at substantially at the same time through the sync circuit, and b) including another sync circuit and each of the sync circuit includes a capacitance.

Parker et al. discloses, in Fig. 2, a) a sync circuit [54,50], which is (i) operably coupled between first and second paths [(30,32,34, 36);(38,40, 42)], (ii) configured to synchronize the speed of signals traveling on the two paths to arrive at the output driver by bi-directionally synchronizing the two paths through the sync circuit *(by regulating the delay difference imposed*

by an unequal number of inverters; see col. 3, lines 22-52), and b) another sync circuit [44,46] and each sync circuit includes a capacitance *(It is well-known in the art that inverters do have capacitance (see U.S. 6,107,847, col.7, lines 31-32))*.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the differential output structure of the Applicant's Admitted Prior Art (Fig. 1) by additionally configuring a sync circuit and an additional sync circuit between the first and second paths of the differential output structure of the Applicant's Admitted prior Art (Fig. 1) as taught by Parker et al. to overcome the delay difference imposed by an unequal number of inverters between the two paths since such an arrangement of the sync circuit for the stated purpose has been a well known practice in the art as evidenced by the teachings of Parker et al. *(see Parker et al.; col. 3, lines 22-52)*.

With respect to claim 31, the Applicant's Admitted Prior Art (Fig. 1) discloses that (1) the first path further includes a plurality of driving elements [12, 16, 18] connected in series to one another, and provides an inverted *(inverted/non-inverted is counted through inverters 12, 16, 18)* output [D] of the input signal, and (2) the second path includes a plurality of driving elements [26, 28] being connected in series to one another, and provides a non-inverted *(inverted/non-inverted is counted through inverters 12, 16, 18)* output [F] of the input signal.

With respect to claim 32, the Applicant Admitted Prior Art (Fig. 1) discloses that the driving elements of the first (12, 16, 18) and second (26, 28) paths have a predetermined constant taper ratio *(indicated in the driving elements)*.

With respect to claim 33, the Applicant Admitted Prior Art (Fig. 1) discloses that each sync circuit is coupled between an output of a driving element on the first path having a first

current driving capability and an output of a driving element on the second path having a second current driving capability, and wherein the first current driving capability is greater than the second current driving capability.

With respect to claim 37, the combination of Applicant Admitted Prior Art (Fig. 1) and Parker et al. (Fig. 3) discloses a sync circuit [50, 54], which is (i) operably coupled between first and second paths, and (ii) configured to synchronize the speed of signals traveling on the two paths. Fig. 2 of Parker et al. show that the sync circuit [44,46] is coupled between the output ends of the first and second paths.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen

Examiner
Art Unit 2816

LMN